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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	4

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,830	YOUNG, B. ARLEN	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,659,690 to Stuber et al. ("Stuber") in view of knowledge commonly known in the art.

3. In reference to Claim 1, Stuber teaches a method for accessing hardware I/O control blocks, which are stored in an hardware I/O control block array, by a parallel SCSI host adapter (See Column 18 Lines 23-24); and addressing pages containing I/O control blocks using a pointer (See Column 18 Lines 39-46). Stuber does not teach that each page contains a plurality of storage sites for hardware I/O control blocks; addressing one page in a plurality of pages of said hardware I/O control block array for said parallel SCSI host adapter using a first portion of a hardware I/O control block array pointer in said parallel SCSI host adapter; and addressing a hardware I/O control block stored in said one page using a second portion of said hardware I/O control block array

pointer in said parallel SCSI host adapter. The Examiner takes Official Notice that the use of paging in which an address is divided into a first portion representing a page number, and a second portion representing a location in the page, thus allowing multiple objects to be on the same page, is well known in the art, as evidenced by The Free On-Line Dictionary of Computing ("FOLDOC") (See entry 'paging'). US Patent Number 4,374,417 to Bradley et al. ("Bradley") further teaches using a paging system as a means for extending addressing capability by using a page number and an index into the page (See Abstract and Column 1 Lines 9-19). US Patent Number 4,805,097 to De Sanna ("De Sanna") further teaches using paging to require only the portion being executed to be present and allows the other pages to be stored wherever space permits (See Column 1 Line 38 – Column 2 Line 19). US Patent Number 6,434,685 to Sexton et al. ("Sexton") further teaches storing multiple objects on a page which are addressed by a page number and an offset into the page (See Column 2 Lines 1-15 and Column 6 Lines 32-57). Further, it is well known in the art that a pointer is an address, as evidenced by FOLDOC (See entry 'pointer').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 1, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

4. In reference to Claim 2, Stuber teaches the limitations as applied to Claim 1 above. Stuber further teaches that for tagged commands, the number of SCB's to the same target/channel/LUN may equal the space in the SCB array (See Column 19 Lines 44-46), and therefore the tag inherently corresponds to a unique address of the SCB in the array for a reconnecting device (See Column 19 Lines 38-49). Therefore, the tag is inherently used to indicate the location of the hardware I/O control block, and functions in a matter equivalent to the second portion of the hardware I/O control block array pointer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 2, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

5. In reference to Claim 3, Stuber teaches the limitations as applied to Claim 1 above. Stuber further teaches a reconnecting target providing a sequencer with its target and LUN addresses (See Column 119 Lines 56-60). Because the sequencer must search the entire SCB array with the target and LUN addresses until it finds a match, it must inherently store said addresses (See Column 119 Lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using

the well-known technique of paging, resulting in the invention of Claim 3, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

6. In reference to Claim 4, Stuber teaches the limitations as applied to Claim 3 above. Stuber further teaches comparing the reconnecting target and LUN addresses stored in the sequencer with the target and LUN addresses of the SCB's in the SCB array (See Column 119 Lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 4, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

7. In reference to Claim 5, Stuber teaches the limitations as applied to Claim 4 above. Stuber further teaches continuing the SCB and loading the information in the SCB upon determining that the reconnecting target and LUN addresses stored in the sequencer and the target and LUN addresses of the SCB are equal (See Column 119 Lines 60-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 5, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

8. In reference to Claim 11, Stuber teaches a method for accessing hardware I/O control blocks, which are stored in a hardware I/O control block array, by a parallel SCSI host adapter (See Column 18 Lines 23-24); and addressing pages containing I/O control blocks using a pointer (See Column 18 Lines 39-46). Stuber does not teach that said hardware I/O control block array pointer includes a page identifier and a storage site identifier. The Examiner takes Official Notice that the use of paging in which an address is divided into a first portion representing a page number, and a second portion representing a location in the page, thus allowing multiple objects to be on the same page, is well known in the art, as evidenced by FOLDOC (See entry 'paging'). Bradley further teaches using a paging system as a means for extending addressing capability by using a page number and an index into the page (See Abstract and Column 1 Lines 9-19). De Sanna further teaches using paging to require only the portion being executed to be present and allows the other pages to be stored wherever space permits (See Column 1 Line 38 – Column 2 Line 19). Sexton further teaches storing multiple objects on a page which are addressed by a page number and an offset

into the page (See Column 2 Lines 1-15 and Column 6 Lines 32-57). Further, it is well known in the art that a pointer is an address, as evidenced by FOLDOC (See entry 'pointer').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 11, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

9. In reference to Claim 12, Stuber teaches the limitations as applied to Claim 11 above. Stuber does not teach configuring said page identifier to identify a page in said paged hardware I/O control block array so that said paged hardware I/O control block array pointer addresses one hardware I/O control block page in said array. As described in reference to Claim 11 above, pages in a memory system are accessed by splitting the address into a page number, as represented by the most significant bits of the address, and an offset within that page, as represented by the least significant bits of the address, in order to allow multiple items to be stored on a page is well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 12, in order to

extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

10. In reference to Claim 13, Stuber teaches the limitations as applied to Claim 12 above. Stuber further teaches that for tagged commands, the number of SCB's to the same target/channel/LUN may equal the space in the SCB array. The tag is then used to match the correct target/channel/LUN upon reconnection (See Column 19 Lines 44-49). Therefore, the tag is inherently used to indicate the location of the hardware I/O control block, and functions in a matter analogous to the storage site identifier of the hardware I/O control block array pointer. Stuber further teaches that the sequencer compares the tag to SCBs currently stored in the array, and thus the tag value is inherently stored (See Column 19 Lines 46-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 13, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

11. In reference to Claim 14, Stuber teaches the limitations as applied to Claim 13 above. Stuber further teaches comparing the reconnecting target and LUN addresses

stored in the sequencer with the target and LUN addresses of the SCB's in the SCB array (See Column 119 Lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 14, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

12. In reference to Claim 15, Stuber teaches the limitations as applied to Claim 14 above. Stuber further teaches retrieving the SCB upon determining that the reconnecting target and LUN addresses stored in the sequencer and the target and LUN addresses of the SCB are equal (See Column 119 Lines 60-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 15, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

13. In reference to Claim 16, Stuber teaches a sequencer (See Figure 4 Number 320 and Column 2 Lines 53-55); and a memory including a hardware I/O control block array

(See Figure 2 Numbers 240 and 243 and Column 9 Lines 17-23), accessing hardware I/O control blocks, which are stored in a hardware I/O control block array, by a parallel SCSI host adapter (See Column 18 Lines 23-24); and addressing pages containing I/O control blocks using a pointer (See Column 18 Lines 39-46). Stuber does not teach a paged hardware I/O control block array pointer coupled to said sequencer and to said memory; said hardware I/O control block array being paged; and a plurality of pages going from lowest page to highest page. Stuber teaches storing the control blocks on a page. The Examiner takes Official Notice that the use of paging in which an address is divided into a first portion representing a page number, and a second portion representing a location in the page, thus allowing multiple objects to be on the same page, is well known in the art, as evidenced by FOLDOC (See entry 'paging'). Bradley further teaches using a paging system as a means for extending addressing capability by using a page number and an index into the page (See Abstract and Column 1 Lines 9-19). De Sanna further teaches using paging to require only the portion being executed to be present and allows the other pages to be stored wherever space permits (See Column 1 Line 38 – Column 2 Line 19). Sexton further teaches storing multiple objects on a page which are addressed by a page number and an offset into the page (See Column 2 Lines 1-15 and Column 6 Lines 32-57). Further, it is well known in the art that a pointer is an address, as evidenced by FOLDOC (See entry 'pointer'). Stuber further teaches that the available space in the SCB array is equal to the number of unique tags that can be returned upon reconnection of a target (See Column 19 Lines 44-49). The SCB array of Stuber is equivalent to a single page of a paged system,

specifically, the page currently paged-in. Therefore, Stuber teaches the number of hardware I/O block storage sites on one of the pages is equal to the number of unique tag values that can be returned by a tagged queue SCSI target reconnecting to said parallel SCSI host adapter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 16, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

14. In reference to Claim 17, Stuber teaches the limitations as applied to Claim 16 above. Stuber does not teach that the memory is external to the parallel SCSI host adapter. Stuber does teach a memory that is internal to the parallel SCSI host adapter (See Figure 4 Number 340). The invention of Claim 17 would perform equally well with an internal memory, as in the prior art. Both the external memory and the internal memory accomplish the same result, viz. providing a storage means for the hardware I/O control block array. The external memory appears to offer no advantage over the prior art's internal memory and therefore it makes no difference which arrangement is used. Further, the mere fact that a structure is integral does not preclude its consisting of various elements.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 17, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

15. In reference to Claim 18, Stuber teaches the limitations as applied to Claim 16 above. Stuber further teaches a memory that is internal to the parallel SCSI host adapter (See Figure 4 Number 340).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the hardware I/O control block array of Stuber using the well-known technique of paging, resulting in the invention of Claim 18, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

16. In reference to Claim 19, Stuber teaches an expanded SCSI control block array for a parallel SCSI host adapter (See Figure 4 Number 443); and a plurality of SCSI control block storage sites (See Column 18 Lines 11-12). Stuber does not teach a plurality of pages going from lowest page to highest page. Stuber teaches storing the control blocks on a page (See Column 18 Lines 11-12 and Column 18 Lines 39-46).

The availability of only four active control blocks causes I/O bottlenecks in several situations. The Examiner takes Official Notice that the use of paging in which an address is divided into a first portion representing a page number, and a second portion representing a location in the page, thus allowing multiple objects to be on the same page, is well known in the art, as evidenced by FOLDOC (See entry 'paging'). Bradley further teaches using a paging system as a means for extending addressing capability by using a page number and an index into the page (See Abstract and Column 1 Lines 9-19). De Sanna further teaches using paging to require only the portion being executed to be present and allows the other pages to be stored wherever space permits (See Column 1 Line 38 – Column 2 Line 19). Sexton further teaches storing multiple objects on a page which are addressed by a page number and an offset into the page (See Column 2 Lines 1-15 and Column 6 Lines 32-57). Further, it is well known in the art that a pointer is an address, as evidenced by FOLDOC (See entry 'pointer'). Stuber further teaches that the available space in the SCB array is equal to the number of unique tags that can be returned upon reconnection of a target (See Column 19 Lines 44-49). The SCB array of Stuber is equivalent to a single page of a paged system, specifically, the page currently paged-in. Therefore, Stuber teaches the number of hardware I/O block storage sites on one of the pages is equal to the number of unique tag values that can be returned by a tagged queue SCSI target reconnecting to said parallel SCSI host adapter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the SCSI control block array of Stuber using the well-

known technique of paging, resulting in the invention of Claim 19, in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

17. Claims 6, 7, 8, 9, and 10, is rejected under 35 U.S.C. 103(a) as being unpatentable over Stuber and knowledge commonly known in the art, as applied to Claim 4 above, and further in view of US Patent Number 6,373,737 to Lysinger et al. ("Lysinger").

18. In reference to Claim 6, Stuber and knowledge commonly known in the art teach the limitations as applied to Claim 4 above. Stuber does not teach changing said first portion of said hardware I/O control block array pointer upon said target address and said reconnecting target address being unequal. Lysinger teaches a content-addressable memory wherein the address currently being compared in a memory module is changed upon determination that the data at that address does not match the data being compared to it (See Column 1 Lines 66-67 and Column 2 Lines 1-4). Content-addressable memories are known in the art to be commonly used in paged-memory systems, as evidenced by FOLDOC (See entries 'content addressable memory' and 'Memory Management Unit').

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber using the well-known technique of paging with the content

addressable memory of Lysinger, resulting in the inventions of Claim 6, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).

19. In reference to Claims 7 and 8, Stuber and knowledge commonly known in the art and Lysinger teach the limitations as applied to Claim 6 above. Stuber does not teach addressing another page in said plurality of pages of said hardware I/O control block array for said parallel SCSI host adapter using a first portion of a hardware I/O control block array pointer in said parallel SCSI host adapter wherein said one page includes a plurality of storage sites for hardware I/O control blocks; and addressing a hardware I/O control block stored in said one page using a second portion of said hardware I/O control block array pointer in said parallel SCSI host adapter. As shown in Claim 1 above, the use of paging in which an address is divided into a first portion representing a page number, and a second portion representing a location in the page, thus allowing multiple objects to be on the same page, is well known in the art. Further, it is well known in the art that a pointer is an address, as evidenced by FOLDOC (See entry 'pointer'). Stuber further does not teach that the page being addressed is another page in the plurality of pages of said hardware I/O control block array. As in Claim 6 above, Lysinger teaches that the address currently being compared in a memory module is changed upon determination that the data at that address does not match the data being compared to it (See Column 1 Lines 66-67 and Column 2 Lines 1-4).

Because the address is changed, the device of Stuber will be operating on a different page.

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber using the well-known technique of paging with the content addressable memory of Lysinger, resulting in the inventions of Claims 7 and 8, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).

20. In reference to Claim 9, Stuber and knowledge commonly known in the art and Lysinger teach the limitations as applied to Claim 8 above. As in Claim 4, Stuber further teaches comparing the reconnecting target and LUN addresses stored in the sequencer with the target and LUN addresses of the SCB's in the SCB array (See Column 119 Lines 56-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber using the well-known technique of paging with the content addressable memory of Lysinger, resulting in the inventions of Claim 9, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).

21. In reference to Claim 10, Stuber and knowledge commonly known in the art and Lysinger teach the limitations as applied to Claim 9 above. As in Claim 5, Stuber further teaches retrieving the SCB upon determining that the reconnecting target and LUN addresses stored in the sequencer and the target and LUN addresses of the SCB are equal (See Column 119 Lines 60-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber using the well-known technique of paging with the device of Lysinger, resulting in the inventions of Claim 10, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).

Response to Arguments

22. In response to Applicant's traversal of the Official Notice taken by the Examiner in rejecting Claims 1, 11, 16, and 19, the Examiner further cites US Patent Number 4,374,417 to Bradley et al. ("Bradley"), US Patent Number 4,805,097 to De Sanna ("De Sanna"), and US Patent Number 6,434,685 to Sexton et al. ("Sexton") as further proof that paging was well known in the art at the time the invention was made. Bradley teaches using a paging system as a means for extending addressing capability by using a page number and an index into the page (See Abstract and Column 1 Lines 9-19). De Sanna teaches using paging to require only the portion being executed to be present

and allows the other pages to be stored wherever space permits (See Column 1 Line 38 – Column 2 Line 19). Sexton teaches storing multiple objects on a page which are addressed by a page number and an offset into the page (See Column 2 Lines 1-15 and Column 6 Lines 32-57). Examiner notes that paging does not require multiple disks, but can be used as a means for extending the address space, and thus the use of paging can be applied to a system in which the plurality of pages is in the hardware I/O control block array. Examiner further notes that the claims and the specification do not preclude further pages from being located outside of the array. Therefore, even if the method of paging used required multiple disks, the pages currently in the active disk would be addressed in the same manner as any pages outside of the active disk, since pages currently "paged in" are addressed in the same manner as pages currently "paged out",

Applicant has further argued that inherent properties of the invention disclosed in the disclosure have not been considered. However, the properties to which the Applicant refers to are not inherent properties of the invention, but are merely possibilities. By definition, inherency is an essential constituent or characteristic. That all SCSI targets can be supported at the same time does not mean that all SCSI targets must be supported at the same time. That no special hardware assistance is required does not preclude providing special hardware assistance. That no lookup tables are required to convert the tag does not preclude using lookup tables to convert the tag. That very little time is required does not provide an indication as to how long "very little time" is.

23. In reference to Claim 2, Applicant has argued that the portion of Stuber cited by the Examiner teaches nothing about addressing a location in an SCB array. However, as noted in the rejection above, the number of SCB's to the same target/channel/LUN may equal the space in the SCB array (See Column 19 Lines 44-46), and therefore the tag inherently corresponds to a unique address of the SCB in the array for a reconnecting device (See Column 19 Lines 38-49). Thus, the tag functions in an equivalent manner to the second portion of the pointer.

24. In reference to Claim 19, Applicant has further argued that the Examiner rejected "hardware I/O control blocks" and not "SCSI control block storage sites." The Examiner notes that a "SCSI control block" is a "hardware I/O control block" and the terms "SCSI control block" and "SCSI control block storage site" are used throughout the rejection over Stuber, whose invention deals with SCSI control blocks.

25. In reference to Claim 6, Applicant has argued that Stuber would not work with the content addressable memory of US Patent Number 6,373,737 to Lysinger ("Lysinger") because Stuber teaches walking the SCB array to find a match. However, Lysinger teaches comparing a value in the array with an input signal representing the sought after value, and sequentially changing the address to the next location in the array, which is equivalent to walking through the array, and comparing that value with the input

signal (See Column 1 Line 66 – Column 2 Line 9). This continues until the sought after value is found or the end of the array is reached.

26. Applicant has argued that dependent claims 2-10, 13-15, and 17-18 are allowable due to their dependence on Claims 1, 11, and 16. However, as shown in the rejections above, Claims 1, 11, and 16 do not distinguish over the prior art and thus the rejections of Claims 2-10, 13-15, and 17-18 are maintained.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-

5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TJC

Thomas J. Cleary
Patent Examiner
Art Unit 2111